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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,756	02/23/2004	John McKenna Brennan	5-84-2-6 2203	
7590 05/17/2005			EXAMINER	
Ryan, Mason & Lewis, LLP			PAREKH, NITIN	
90 Forest Avenue Locust Valley, NY 11560			ART UNIT	PAPER NUMBER
			2811	
		DATE MAILED: 05/17/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
	10/784,756	BRENNAN ET AL.	
Office Action Summary	Examiner	Art Unit	
	Nitin Parekh	2811	
The MAILING DATE of this communication app Period for Reply	pears on the cover sheet with the c	orrespondence address	
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION.  Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication.  If the period for reply specified above is less than thirty (30) days, a repl  If NO period for reply is specified above, the maximum statutory period of Failure to reply within the set or extended period for reply within the set or extended period for reply with by statute Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	I36(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) day will apply and will expire SIX (6) MONTHS from e, cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).	
Status			
Responsive to communication(s) filed on <u>02 №</u> This action is <b>FINAL</b> . 2b)  This 3) Since this application is in condition for alloward closed in accordance with the practice under №	s action is non-final. nce except for formal matters, pro		
Disposition of Claims			
4) Claim(s) 1-20 is/are pending in the application 4a) Of the above claim(s) is/are withdra 5) Claim(s) is/are allowed. 6) Claim(s) 1-20 is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or Application Papers	wn from consideration.		
9) The specification is objected to by the Examine 10) The drawing(s) filed on 23 February 2004 is/ar Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11) The oath or declaration is objected to by the Examine 11.	e: a) ☐ accepted or b) ☒ objecte drawing(s) be held in abeyance. Sec ction is required if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).	
Priority under 35 U.S.C. § 119			
a) All b) Some * c) None of:  1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Burea * See the attached detailed Office action for a list	ts have been received. ts have been received in Applicationity documents have been received in (PCT Rule 17.2(a)).	on No ed in this National Stage	
Attachment(s)  1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 04-05-04.	4) Interview Summary Paper No(s)/Mail D  5) Notice of Informal F 6) Other:		

#### **DETAILED ACTION**

1. Applicant's election with traverse of claims of Group I in the reply filed on 05-04-04 is acknowledged. The restriction requirement set forth in the previous office action is withdrawn based on the arguments in response to the restriction requirement.

### **Drawings**

2. Figures 1A/1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 1, 2, 5-10, 14 and 17-20 are rejected under 35 U.S.C. 102(b) as being 4. anticipated by Joshi et al. (US Pat. 5955781).

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Regarding claims 1, 2 and 5 and 10, Joshi et al. disclose a semiconductor device (see Fig. 3) and a method/steps of making such device comprising:

- a semiconductor/silicon substrate (106 in Fig. 3)
- an active region formed in the substrate proximate an upper surface of the substrate (see device/gate-junctions region in Fig. 3), the active region including at least one circuit element formed therein
- a plurality of trenches/channels (108 in Fig. 3) formed in a back surface of the substrate opposite the upper surface of the substrate, the trenches /channels being formed proximate the active region
- the trenches/channels being substantially planar with the back surface of the substrate, and
- wherein the trenches/channels are filled with a thermally conductive material/TCM (see 102 in Fig. 3) such as diamond, the TCM having a thermal conductivity (TC) being greater than that of the substrate (see Table 1) and being configured so as to provide a thermal conduction path for conducting heat away from the active region (Col. 5, line 60- Col. 6, line 5)

(Fig. 3; Col. 4, line 15- Col. 6, line 5; Col. 1-8).

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Regarding claims 6- 9, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach:

the trenches/channels comprising substantially v-shaped grooves having sloped sidewalls (see Fig. 2C; Col. 5, lines 25-52), and

- the trenches/channels being formed using an etching process comprising anisotropic etching (Col. Col. 5, line 65; Col. 6, line52; Col. 8, lines 25-28).

Regarding claim 14, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the device structure comprising a plurality of active devices/regions being formed in the upper surface of the substrate such that each of the trenches/channels are proximate a corresponding one of the active devices/regions to provide the desired heat dissipation for the structure (Col. 2, lines 60-65).

Regarding claims 17-19, Joshi et al. disclose the steps/method of forming the device as applied to claim 1 above.

Regarding claim 20, Joshi et al. disclose the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the device structure comprising a cooling tower/base (120 in Fig. 5) wherein an integrated circuit die/chip (122 in Fig. 5) is attached to the base to provide a thermal conduction path between the active region

and the base for conducting heat away from the active region (Fig. 3 and 5; Col. 6, lines 16-25).

## Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 3, 4, 11, 12, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US Pat. 5955781)

Regarding claims 3, 4 and 12, Joshi et al. teach the entire structure as applied to claim 1 above, except the TCM comprising a metal or at least one of copper, aluminum, gold, silver, a copper alloy, and an aluminum alloy.

Joshi et al further teach using TCM including metals such as tungsten, copper, aluminum, etc. (see Col. 6, lines 43-47; Col. 7, lines 25-27) to provide improved heat dissipation for the device. Furthermore, the metal such as tungsten has a coefficient of thermal expansion (CTE) substantially matching to that of the substrate (see Table 1).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the TCM comprising a metal or at least one of

copper, aluminum, gold, silver, a copper alloy, and an aluminum alloy in the channel so that the device processing can be simplified and the material handling/cycle time can be improved in Joshi et al's device.

Regarding claim 11, Joshi et al. teach the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the trenches/channels having the TCM being formed in the selected regions or the region adjacent or alongside/lengthwise the active regions of the device (Col. 7, lines 5-9; Col. 8, line 26), but fail to teach at least one channel being formed through a length of the device between opposing sides of the device.

The determination of parameters such as size/dimension including length/width, height, thickness, spacing, etc. of the active region/source-gate-drain, metal interconnect, thermally conductive via/plug, substrate/heat sink/thermally conductive structure, etc. in chip packaging and interconnect technology is a subject of routine experimentation and optimization to achieve the desired thermal/electrical performance, speed, reliability and yield.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select at least one channel being formed through a length of the device between opposing sides of the device so that the thermal dissipation can be improved in Joshi et al's device.

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Regarding claims 15 and 16, Joshi et al. teach the entire structure as applied to claim 1 above, wherein Joshi et al. further teach the trench/channel being approximately 2-10 microns from a surface of the substrate (see Fig. 2C), but fail to teach at least one channel being formed having a maximum height that is about two thousandths of an inch from the upper surface of the substrate or about forty micrometers from the active region.

The determination of parameters such as size/dimension including length/width, height, spacing, etc. of the active region/source-gate-drain, metal interconnect, thermally conductive via/plug, substrate/ thickness, etc. in chip packaging and interconnect technology is a subject of routine experimentation and optimization to achieve the desired thermal/electrical performance, speed, reliability and yield.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select at least one channel being formed having a maximum height that is about two thousandths of an inch from the upper surface of the substrate or about forty micrometers from the active region so that the desired thermal dissipation, electrical performance can be achieved and the reliability/yield can be improved in Joshi et al's device.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (US Pat. 5955781) in view of the admitted prior art (APA).

Regarding claims 13, Joshi et al. teach the entire structure as applied to claim 1 above, except the device having a cross-sectional thickness greater than or equal to about six thousandths of an inch.

The APA teaches devices having six mils or more (specification pp. 1)

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the device having a cross-sectional thickness greater than or equal to about six thousandths of an inch as taught by the APA so that warpage can be reduced in Joshi et al's device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

NITIN PAREKH

05-11-05

PRIMARY EXAMINER

**TECHNOLOGY CENTER 2800**